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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,116	12/01/2003	Rahul Magoon	26169-103-401	9927

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,116	MAGOON ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janc et al U.S. patent No 4,785,463 in view of Schenck et al U.S. Patent No 6,445,229 B1.

As per claims 1, 10 and 19, Janc et al disclose a method of generating at least two modulation signals from a local oscillator signal for quadrature sub-harmonic modulation of a quadrature amplitude modulated information signal (see fig.8), such method comprising the steps of: delaying (see fig.8 element 878 and col.17, lines 35-67) the local oscillator signal (see fig.8 element 846 and col.17, line 21 and col.18, lines 20-31) at least two sets of modulator signals, one of said sets of modulator signals together forming the first modulation signal (see fig.8 element 802) and another of said sets forming the second modulation signal (see fig.8 element 822) for quadrature sub-harmonic modulation of the quadrature amplitude modulated information signal.

However Janc et al does not teach delaying the local oscillator <u>in a plurality of incremental delay steps to form and controlling a magnitude of the incremental delays based upon a predetermined phase offset between the local oscillator signal and a last delay step of the incremental delay steps.</u>

Schenck et al teaches delaying the local oscillator in a plurality of incremental delay steps (see figs.1, 3-5, 9 elements 16, 20, 44 and col.3, lines 5-15 and col.4, lines 25-30) to form and controlling (see figs.1, 4 elements 24, 42 and col.3, lines 10-30 and col.4, lines 8-32) a magnitude of the incremental delays based upon a predetermined phase offset between the local oscillator signal and a last delay step of the incremental delay steps.

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Schenck into Janc as to generate timing for both the logical high phases and logical low phases series of the clock cycles and produce consistent incremental delays in order to avoid use of amplifiers which could cause current spikes as taught by Schenck (see col.1, lines 50-67).

As per claims 2, 11 and 20, Janc does include the first modulation signal as a real part of the quadrature sub harmonic modulation signal (see fig.8 and col.6, lines 40-67 and col.7, lines 55-67).

As per claims 3, 12 and 21, Janc does include the second modulation signal as an imaginary part of the quadrature sub harmonic modulation signal (see fig.8 and col.10, lines 36-43).

As per claims 4, 13 and 22 Janc includes the delay of each delay step as substantially equal to ninety degrees divided by a modulator multiplier value (see fig.8).

As per claims 5, 14 and 23, Janc does include the first and second modulation signals as having a number of respective odd and even members (see col.11, lines 40-42) equal to two times the modulator multiplier value.

As per claims 6, 15 and 24Janc would include a first incremental delay step as equal to zero degrees as to produce consistent incremental delays in order to avoid use of amplifiers which could cause current spikes.

As per claims 7, 16 and 25 Janc would include defining a second incremental delay step as equal to forth-five degrees as to produce consistent incremental delays in order to avoid use of amplifiers which could cause current spikes.

As per claims 8, 9, 17, 18 and 26-27, Janc would include defining a third incremental odd delay step as equal to ninety degrees as to produce consistent incremental delays in order to avoid use of amplifiers which could cause current spikes

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 28 is rejected under 35 U.S.C. 102(b) as being anticipated by Schulz et al U.S. patent No 5,053,717.

As per claim 28, Schulz et al teaches a method of providing first and delayed second modulator signals for modulation of a quadrature amplitude modulated signal, such method comprising the steps of: detecting a phase difference relating the first and second modulator signals (see abstract and col.1, lines 55-67 and col.2, lines 15-25); filtering (see fig.2 element 269) the detected phase difference; adjusting (see fig.2 element 259 and col.2, lines 22-24, 63-65 and col.3, lines 65-67) the phase difference between the first and second modulator signal based

upon the filtered, detected phase difference to a phase difference value equal to ninety degrees (see fig.2 element 215) divided by a modulator multiplier value for quadrature sub harmonic modulation of the quadrature amplitude modulated signal.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gossmann et al U.S. patent No 6,359,950 B2 teaches a digital PLL.

Rotzoll U.S. Patent No 5,737,035 teaches a highly integrated television tuner.

Yoshikawa et al U.S. patent No 6,198,415 B1 teaches a serial-to-parallel converter.

Zortea et al U.S. Patent No 6,389,090 B2 teaches a digital clock/data signal recovery.

Dally et al U. S. Patent No 6,316,987 B1 teaches a low-power low jitter variable delay.

Hayase et al U.S. Patent No 6,259,293 b1 teaches a delay circuitry.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 703 308-9573. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 703 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

7/23/04

EMMANUEL BAYARD
PRIMARY EXAMINER